line 14, after "value" insert --;--;
line 15, after "register" insert --;--;
line 16, after "value" insert --;--;
line 17, after "register" insert --; and--;
line 18, after "accumulator" insert --.--;
line 23, delete "a"; change "speed" to --speeds--; after "than" insert --,--; after "instance" insert --,--;
line 24, change "a" to --from--; after "times" insert --improvement--;
line 25, change "faster" to --in--; after "processing" insert --speed--;
line 32, before "annex" insert --an--; and
line 33, after "field" insert --,--.

IN THE DRAWING

Please amend the drawing as indicated in red on the enclosed copy of Figure 1 submitted herewith.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A circuit for processing integer data[,] for graphic image processing applications, comprising:

[-] a multiplier unit <u>having a pipeline</u> for multiplying integer data words[,] of 8 bits or multiples thereof, [in which unit a] <u>the</u> pipeline [forms part and the word length of which is] <u>being</u> adjustable [for the multiplication to be performed in accordance with the multiple of 8 bits for multiplying] <u>to the length of the integer data words to be multiplied</u>;

[-] an arithmetic logic unit (ALU) for performing arithmetic operations on integer data words of 8 bits or multiples thereof, the word length of [which is] <u>the ALU being</u> adjustable in accordance with the multiple of 8 bits [for processing] <u>constituting the integer and data words</u>;

[-] a register unit provided with at least two registers for storage [therein for some time] of the integer data words [of a multiple of 8 bits] on which one of the operation [and/or] and pipeline multiplication has to be performed; and

[-] a bus structure for effecting the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit [which comprises a number], the bus structure having a plurality of separate buses each having a separate register connected thereto for transmitting and receiving the integer data words [and which effects the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit].

2. (Amended) [A] The circuit according to claim 1, wherein the pipeline is a five-step pipeline.

3. (Twice Amended) [A] The circuit according to claim 1, wherein the integer data comprises one of 32 bit words, [or] 16 bit words, and 8 bit words.

4. (Amended) A multiplier unit [with] having a pipeline[, the] and a variable length accumulator, the multiplier having a word length [of] which is adjustable [for] and the multiplication [to be] is performed in accordance with the length of [the] integer data words [for] being [multiplying, of] multiplied, the length of the integer data words being 8 bits or a multiple thereof.

5. (Amended) An arithmetic logic unit comprising a plurality of partitioned arithmetic logic units therein, the word length of the arithmetic logic unit being [which is] adjustable in accordance with the length of the integer data words [for processing of] being processed, the length of the integer data words being 8 bits [words] or multiples thereof.

6. (Amended) A shift register unit having control logic capable of receiving an integer data word having a length which is variable in increments of 8 bits, the shift register unit for shifting a 32 bit integer data word through a distance of 1 to 32 bits [to the] , in one of a left [or the] and a right direction and in one of a rotating [or] and a non-rotating manner.

Claim 7, line 1, change "A" to --The--.

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8. (Twice Amended) The circuit as claimed in claim 1, further comprising an instruction register, wherein the bus structure is provided with a [number] plurality of registers [or other connections] and wherein [these connections are programmable from an instruction register] the transport of the integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmable from the instruction register.

Claim 10, line 1, change "A" to --The--.

Claim 11, line 1, change "A" to --The--.

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12. (Amended) The circuit as claimed in claim 2, further comprising an instruction register, wherein the bus structure is provided with a [number] plurality of registers [or other connections] and wherein [these connections are programmable from an instruction register] the transport of the integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmable from the instruction register.

13. (Amended) The circuit as claimed in claim 3, further comprising an instruction register, wherein the bus structure is provided with a [number] plurality of registers [or other connections] and wherein [these connections are programmable from an instruction register] the transport of the

integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmable from the instruction register.

14. (Amended) The circuit as claimed in claim 7, further comprising an instruction register, wherein the bus structure is provided with a [number] plurality of registers [or other connections] and wherein [these connections are programmable from an instruction register] the transport of the integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmable from the instruction register.

Please add the following new claims:

15. A circuit for processing digital data words, comprising:

a multiplier unit for multiplying the digital data words, the multiplier unit having a pipeline in which the word length is adjustable to match the length of the digital data words, the digital data having a length which varies incrementally;

an arithmetic logic unit (ALU) capable of performing arithmetic operations on the digital data words, the ALU being adjustable to match the length of the digital data words;

a register unit having at least two registers for storage of the digital data words; and

a bus structure for transporting the digital data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure having a plurality of separate buses each having a register connected thereto for transmitting and receiving the digital data words.

16. The circuit according to claim 15, wherein the pipeline is a five-step pipeline.

17. The circuit according to claim 15, wherein the multiplier unit further comprises a Wallace tree.